Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. **(Original)** A memory system that is configured with a plurality of memory controllers (SCx) disposed in parallel on a clocked bus (B) and memory chips (Fx) associated with the respective memory controllers (SCx), and that communicates via the bus (B) with a host system (HS) by means of operational memory commands using logical memory sector numbers, characterized in that in the case of a memory operation requested by the host system (HS), the memory controller (SCx) affected with respect to a range of logical memory sector numbers takes over the bus for the communication with the host system (HS) by means of arbitration.

2. **(Original)** A memory system according to claim 1, characterized in that one of the parallel memory controllers (SCx) is designated as the master (M) on the bus (B) and that it performs the communication with the host system (HS) as long as none of the other memory controllers (SCx) has taken over the bus (B).

3. **(Original)** A memory system according to claim 1, characterized in that the arbitration of the bus (B) between the memory controllers (SCx) takes place

based on the addressed memory sector number and over a single tri-state line (BA) that indicates the reservation of the bus (B) by the affected memory controller (SCx) during the communication period with a "reserved" signal.

4. **(Original)** A memory system according to claim 3, characterized in that when the bus (B) is released by a memory controller (SCx), a shield time is inserted on the arbitration line (BA), during which the line (BA) is actively driven to "released".

5. **(Original)** A memory system according to claim 4, characterized in that the shield time corresponds to the length of one clock cycle of the bus (B).

6. **(Original)** A memory system according to claim 1, characterized in that for consecutive logical memory sector numbers different memory controllers (SCx) are assigned.

7. **(Original)** A memory system according to claim 1, characterized in that the memory chips (Fx) are flash memories that are erasable in blocks.

8. **(Previously Presented)** A memory system according to claim 1, characterized in that the memory controllers (SCx) are jointly disposed on a semiconductor substrate (H).

9. **(Original)** A memory system according to claim 8, characterized in that the designation of the sequence of the memory controllers (SCx) on the bus (B) and of the master (M) takes place by means of programming a control register (KR) to the respective memory controllers (SCx).

10. **(Currently Amended)** A method for determining ~~the~~ a sequence of the memory controllers (SCx) in a memory system with multiple memory controllers which is operated by a host system (HS) over a ~~on the~~ bus (B) which includes an arbitration line (BA), ~~characterized in that~~comprising:

- after a repeated designation command by the host system (HS), a memory controller (SCx) occupies, after a randomly determined amount of time, the arbitration line (BA) in each case for a specified length of time, provided that no other controller (SCx) has previously reserved the line (BA),
- from the number of repetitions of ~~this~~ the designation command the controller derives its controller number (Sx),
- a confirmation signal is reported to the host system (HS) in each case,
- the respective memory controller (SCx) withdraws from the designation process after the confirmation.

11. **(Original)** A method according to claim 10, characterized in that the memory controller (SCx) with the controller number 1 is designated as the master (M).

12. **(Original)** A method according to claim 10, characterized in that the host system (HS) repeats the designation process if insufficient designation confirmations are reported.

13. **(Original)** A method according to claim 10, characterized in that the random time for occupying the arbitration line (BA) is derived from a counter that is subject to component tolerances.